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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,011	07/07/2003	Masahiko Hosokawa	392.1803	4508

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EXAMINER	
SHECHTMAN, SEAN P	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,011	HOSOKAWA ET AL.	
	Examiner	Art Unit	
	Sean P. Shechtman	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 are presented for examination. Claims 1-3 and 7-11 have been amended.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 9, 11, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 6,173,208 to Park.

Referring to claim 9, Park teaches a numerical controller for controlling a machine according to a machining program (Col. 1, lines 6-27), comprising: a storage device for storing input/output units (Col. 3, lines 18-26) each including program block data obtained by dividing the machining program so that divided portions of the machining program are stored in respective ones of the input/output units (Col. 3, lines 27-33), each input/output units storing additional information associated with the program data stored in the input/output units, said additional information including first link data designating an input/output immediately preceding each input/output unit in a sequence of the machining program and second link data designating an input/output unit following each input/output unit in the sequence of the machining program (Col. 4, lines 48-65); a processor for processing the input/output units to run the divided portions of the machining program stored in the input/output units (Col. 5, lines 24-32; Col. 7, lines 13-19).

Referring to claims 11 and 12, Park teaches said processor deletes/adds an input/output unit by changing rear link data of a preceding input/output unit designated by front link data of the input/output unit to be deleted/added to rear link data of the input/output unit to be

deleted/added, and changing front link data of an input/output unit designated by rear link data of a succeeding input/output unit to be deleted/added to the front link data of the input/output unit to be deleted/added (Col. 5, lines 1-5; Col. 6, lines 13-29).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,298,006 to Miyajima in view of U.S. Pat. No. 5,319,778 to Catino.

Referring to claim 1, Miyajima teaches a numerical controller for controlling a machine according to a machining program (Abstract), comprising: a storage device or medium for storing input/output units (Fig. 3, element 100; Col. 4, lines 45-50), each of the input output units including program block data (Fig. 3, elements P3-P5 store programs 101, 102...), said program block data is obtained by dividing the machining program so that divided portions of the machining program are stored in respective ones of the input/output units (See Fig. 3), each of the input/output units storing additional information associated with the program data stored in the input/output units (Fig. 3, elements P3-P5, start commands beginning with U and end commands beginning with V), said additional information including front input/output unit data designating an input/output unit immediately preceding each input/output unit in a sequence of the machining program (Fig. 3, elements P3-P5, start commands beginning with U) and rear input/output unit data designating an input/output unit following each input/output unit (Fig. 3, elements P3-P5, start commands beginning with U and end commands beginning with V) in a sequence of the machining program (Col. 3, line 66 - Col. 4, line 9); a processor for processing

the input/output units to run the divided portions of the machining program stored in the input/output units (Col. 2, lines 48-56).

Miyajima teaches all of the limitations set forth above, however Miyajima fails to teach that said additional information includes first link data designating an input/output unit immediately preceding each input/output unit and second link data designating an input/output unit following each input/output unit.

However, Catino teaches analogous art, wherein a programming structure at the machine level provides for manipulation of linked lists in data operations (Col. 2, lines 3-7) wherein information in blocks of memory include first link data designating an input/output unit immediately preceding each input/output unit and second link data designating an input/output unit following each input/output unit (Col. 5, line 11 – Col. 6, line 39).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the teachings of Catino with the teachings of Miyajima.

One of ordinary skill in the art would have been motivated to combine these references because Catino teaches manipulation of linked lists in such a way as to allow multiple processes in a parallel computing environment to access shared lists without the need for additional synchronization, wherein there are no restrictions on the location of forward or backward pointers within the linked list elements such that the linked lists can be defined with multiple sets of forward and backward pointers enabling the list elements to reside in multiple lists (Col. 2, lines 3-24).

4. Claims 1-2, 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,173,208 to Park in view of U.S. Pat. No. 6,088,624 to Khan.

Referring to claim 1, Park teaches a numerical controller for controlling a machine according to a machining program (Col. 1, lines 6-27), comprising: a storage device for storing input/output units (Col. 3, lines 18-26) each including program block data obtained by dividing the machining program so that divided portions of the machining program are stored in respective ones of the input/output units (Col. 3, lines 27-33), each input/output units storing additional information associated with the program data stored in the input/output units, said additional information including first link data designating an input/output immediately preceding each input/output unit in a sequence of the machining program and second link data designating an input/output unit following each input/output unit in the sequence of the machining program (Col. 4, lines 48-65); a processor for processing the input/output units to run the divided portions of the machining program stored in the input/output units (Col. 5, lines 24-32; Col. 7, lines 13-19); and an interface for inputting/outputting the input/output units between said storage device or medium and said processor (Cover figure).

Referring to claim 2, Park teaches the controller above, wherein said processor reads a first link data including a program block corresponding to a beginning part of the machining program and successively reads input/output units stored in said storage device or medium according to rear link data in the previously read input/output unit through said interface, and wherein said processor successively executes the program blocks included in the read input/output units (Col. 6, lines 60-62).

Referring to claims 5-8, Park teaches said processor deletes/adds an input/output unit by changing rear link data of a preceding input/output unit designated by front link data of the input/output unit to be deleted/added to rear link data of the input/output unit to be deleted/added, and changing front link data of an input/output unit designated by rear link data of a succeeding input/output unit to be deleted/added to the front link data of the input/output unit to be deleted/added (Col. 5, lines 1-5; Col. 6, lines 13-29).

Park fails to teach that said additional information including an effective data length of the program block. Examiner notes that independent claim 1 does not require that the effective data length be functionally used with respect to any other part of the claim.

However, referring to claim 1, Khan teaches analogous art (Col. 1, lines 18-57 of '624), wherein identifying data structures or its elements within a control program (Col. 2, lines 16-53 of '624) includes software that denotes the size of data of the data elements (Col. 8, lines 1-7 of '624).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to combine the teachings of Khan with the teachings of Park.

One of ordinary skill in the art would have been motivated to combine these references because Khan teaches a method of coordinating memory assigned to both input/output devices of an industrial controller and variables of a control program (Col. 1, lines 13-17 of '624). Furthermore, Khan teaches the ability to adopt arbitrary data structures appropriate to a device, having arbitrary size and divided into arbitrary data types, wherein the invention allows selecting

data structures for exchanging data with a centralized I/O table memory to identify data structures or elements within the control program (Col. 2, lines 17-53 of '624).

5. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,173,208 to Park in view of U.S. Pat. No. 6,088,624 to Khan, as applied to claims 1-2 above, and further in view of U.S. Pat. No. 5,258,905 to Yamauchi. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,173,208 to Park, as applied to claim 9 above, and further in view of U.S. Pat. No. 5,258,905 to Yamauchi.

Referring to claims 3, 4, and 10, Park and Khan teach all the limitations set forth above, however, fail to teach a branch instruction is included in the program block of an input/output unit when it is executed by said processor, said processor reads input/output units preceding the input/output unit being executed using the front input/output unit data and reads input/output units following the input/output unit being executed using the rear input/output unit data to search a line designated by the branch instruction, wherein data specifying an input/output unit including a line designated by a branch instruction, and when the branch instruction is included in the program block of the input/output unit in execution said processor reads the input/output unit specified by the data.

However, referring to claims 3 and 10, Yamauchi teaches analogous art, wherein when a branch instruction is included in the program block of an input/output unit when it is executed by said processor, a processor reads input/output units preceding the input/output unit in execution using the front input/output unit data and reads input/output units following the input/output unit in execution using the rear input/output unit data to search a line designated by the branch

instruction (Col. 6, lines 39-58 of '905). Referring to claim 4, Yamauchi teaches information further includes data specifying an input/output unit including a line designated by a branch instruction, and when the branch instruction is included in the program block of the input/output unit in execution said processor reads the input/output unit specified by the data (Fig. 2b and Fig. 6; Col. 6, lines 39-58 of '905).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to further modify the teaching Park with the teachings of Yamauchi.

One of ordinary skill in the art would have been motivated to combine these references because Yamauchi teaches an expanded programmable machine controller which can independently carry out debugging, operations, and the like, while not connected to the main body programmable machine controller (Col. 1, lines 7-14 of '905).

Response to Arguments

6. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean P. Shechtman whose telephone number is (571) 272-3754. The examiner can normally be reached on 9:30am-6:00pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SPS

Sean P. Shechtman

March 18, 2005

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